Absolute multi-turn shaft encoders BMA/BMB SSI
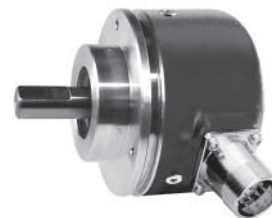
features

- multi-turn encoders up to
  - 13 bit single-turn
  - 12 bit multi-turn
- SSI interface
- Gray and binary code
- self-testing
- counting direction setting input
- zero setting input
- optional: with incremental signals

BMA

BMB

general data

voltage supply	10 - 30 VDC with reverse polarity protection
max. supply current no load	50 mA (at 24 VDC)
max. resolution single-turn multi-turn	13 bit (1 step = 2' 38") 12 bit (4'096 rev.)
max. error limit	±1/2 step
input signal	clock input SSI, F/$\overline{R}$-input, zero set input
max. switching frequency	800 kHz
SSI clock frequency	min. 62,5 kHz up to max. 1,5 MHz (depending on cable length)

mechanical data

|	
max. revolutions	mech. 10'000 rpm electr. 6'000 rpm
moment of interia	2×10^{-6} kgm^2
torque	≤ 0,010 Nm (without sealing ring) ≤ 0,015 Nm (with sealing ring)
max. shaft load	axial: 20 N radial: 40 N
max. protection class	IP 65
material	housing: steel flange: aluminum
weight	approx. 400 g

ambient conditions

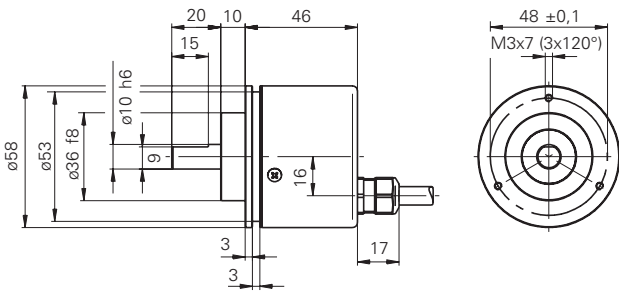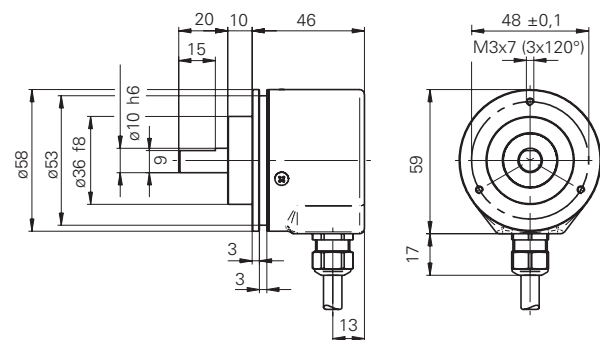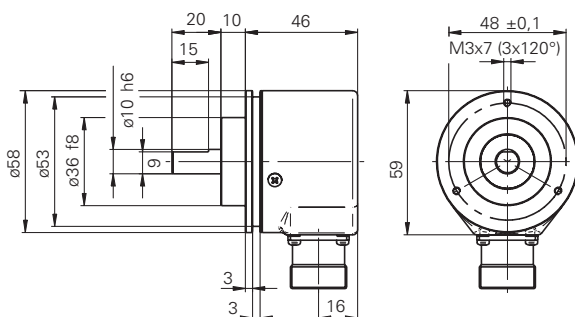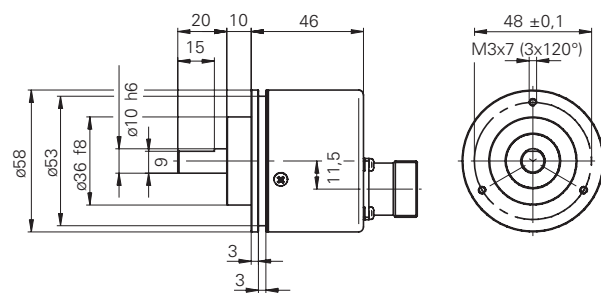|	
temperature range	-25...+85 °C
relative humidity	max. 95% non condensing
vibration	DIN EN 60068-2-6 (≤ 100 m/s^2 / 16 - 2'000 Hz)
shock	DIN EN 60068-2-27 (≤ 2'000 m/s^2 / 6 ms)
noise immunity	DIN EN 61000-6-2
emitted interference	DIN EN 61000-6-4
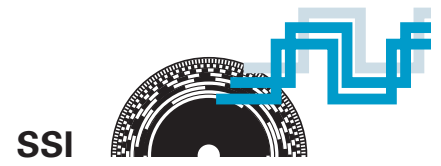
dimensions and connection dimensions

BMA
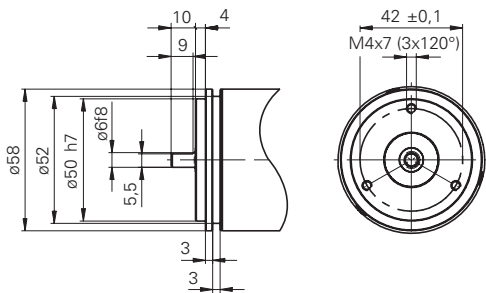
BMB

-4

-5

-A

-B

3

Absolute multi-turn shaft encoders
BMA/BMB
SSI

Designation		
cable	**connector**	**signal (SSI)**
color	**12-pin**	
brown	1	+Vs
black	2	GND
blue	3	clock+
beige	4	data+
green	5	ZERO
yellow	6	data-
violet	7	clock-
brown/yellow	8	$\overline{DV}$
pink	9	F/$\overline{R}$
black/yellow	10	$\overline{DV/MT}$
-	11	-
-	12	-

Screen: In the case of encoders with cable output, the screen is connected to the housing.

## pin assignment M23 male
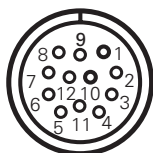
seen from outside

connector 12-pin M23

signals for serial input interface

1 +Vs   Voltage supply connection of the encoder.

2 GND   Ground connection of the encoder. The voltage relating to GND is +Vs.

3 clock+ Clock, together with clock-, forms a current loop. A current of 7 mA in input clockdirection produces a logical 0 in positive logic.

4 data+   Positive, serial data output of the differential ine driver. A HIGH level at the output corresponds to logic 1 in positive logic.

5 ZERO   Zero setting input for setting a zero at any point within the overall resolution. The zero setting process is triggered by a HIGH pulse and should take place after direction of rotation selection (F/$\overline{R}$). Min. signal duration > 100 ms.

6 data-   Negative, serial data output of differential line driver. A HIGH level at the output corresponds to logical 0 in positive logic.

7 clock- Clock-, together with clock, forms a current loop. A current of 7 mA in input clock-direction produces a logical 0 in positive logic.

8 / 10   Diagnosis outputs $\overline{DV}$ and $\overline{DV/MT}$
$\overline{DV}$; $\overline{DV/MT}$ Jumbs in data word, e.g. due to defectiv LED or photoreceiver, are displayed via the $\overline{DV}$ output. In addition, the power supply of the multiturn sensor unit is monitored and the $\overline{DV\ MT}$ output is set when a specified voltage level is dropped below Both outputs are Low-active, i.e. are switched through to GND in the case of an error.

9 F/$\overline{R}$ F/$\overline{R}$ counting direct input. If connected, this input is in HIGH state. F/$\overline{R}$-High means increasing output data with cw shaft rotation. F/$\overline{R}$-Low means increasing output values with ccw shaft rotation, in each case looking at the shaft.
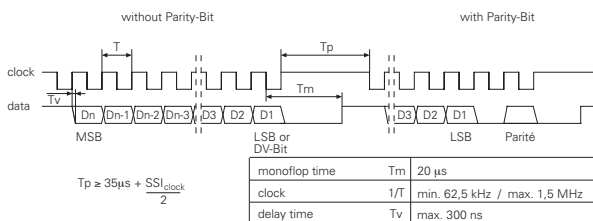
SSI
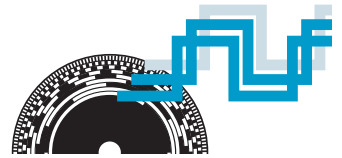
inputs F/R̄ and ZERO

Control signal F/R̄ and ZERO

input voltage	(Vs = 10 - 30 VDC)
HIGH level	> 0,7 - +Vs
LOW level	< 0,3 +Vs

Connection: F/R̄ inputs with 10 kΩ to +Vs for F/R̄, zero setting input with 10 kΩ to GND.

signal characteristic, SSI serial output

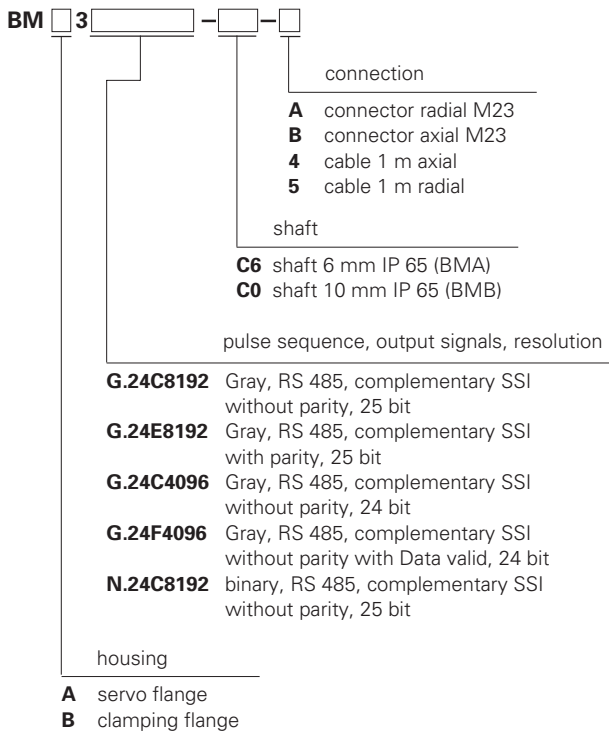without Parity-Bit   with Parity-Bit

clock

data

Dn | Dn-1 | Dn-2 | Dn-3 ... D3 | D2 | D1 ... D3 | D2 | D1

MSB   LSB or DV-Bit   LSB   Parité

$$Tp \geq 35\mu s + \frac{SSI_{clock}}{2}$$

monoflop time	Tm	20 µs
clock	1/T	min. 62,5 kHz / max. 1,5 MHz
delay time	Tv	max. 300 ns

outputs D̄V̄ and D̄V̄/M̄T̄

Outputs push-pull short-circuit protected

HIGH level	> Vs -3,5 V (up to I = -20 mA)
LOW level	≤ 0,5 V (up to I = 20 mA)

accessories

connector 12-Pol M23	part nr. 118319
type BMA servo flange	
mounting	part nr. 125051
scews and servo clamps	part nr. 117668
type BMB clamping flange	
mounting bracket	part nr. 117698

order designation

BM ☐ 3 ☐☐☐☐ – ☐ – ☐

connection

A	connector radial M23
B	connector axial M23
4	cable 1 m axial
5	cable 1 m radial

shaft

C6	shaft 6 mm IP 65 (BMA)
C0	shaft 10 mm IP 65 (BMB)

pulse sequence, output signals, resolution

G.24C8192	Gray, RS 485, complementary SSI without parity, 25 bit
G.24E8192	Gray, RS 485, complementary SSI with parity, 25 bit
G.24C4096	Gray, RS 485, complementary SSI without parity, 24 bit
G.24F4096	Gray, RS 485, complementary SSI without parity with Data valid, 24 bit
N.24C8192	binary, RS 485, complementary SSI without parity, 25 bit

housing

A	servo flange
B	clamping flange

Please use the programmable version of type BMC/BMD for single pieces.

parity bit   reference 24E

For simple error detection during data transmission, an additional parity bit can be transmitted. Two additional clocks are required for transmission (by MT various).

Parity bit = „1" for odd number of HIGH levels in the data word (without parity bit).

Parity bit = „0" for even number of HIGH levels in the data word (without parity bit).

data valid bit (DV)   reference 24F

The D̄V̄ bit can be transmitted instead of the LSB (D1). The maximum single-turn resolution is then reduced to 12 bits.

The transmitted D̄V̄ bit is HIGH active, that is to say if a HIGH level is transmitted, data information is invalid. The data are valid where D̄V̄ bit = LOW.

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